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High Performance Silicon FETs from Ultra-High Density Nanowire Circuits

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SUPPORTING INFORMATION

Calculations of carrier mobilities. Mobilities of all devices were extracted in the linear triode regions with V_{DS}=-0.25V. In this region,[11]

$$\mu = \frac{dI_{DS}}{dV_{GS}} \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}}$$

where $\frac{dI_{DS}}{dV_{GS}}$ is the transconductance and a typical value for our devices is ~1μA/V; L is the device length and is 4 μm; C_{ox} is the gate capacitance and is ~5×10^{-15} F; V_{DS}=0.25 is the source/drain bias.

Extraction of subthreshold swing. Subthreshold swing $S = \frac{dV_{GS}}{d\log(I_{DS})}$ was extracted at current levels below 10^{-10}A, according to literature methods. [2]

Drain current vs. top-gate voltages at different bottom gate potentials. When the top-gate is on, bottom gate modulation is limited and the device is dominated by the top gate.

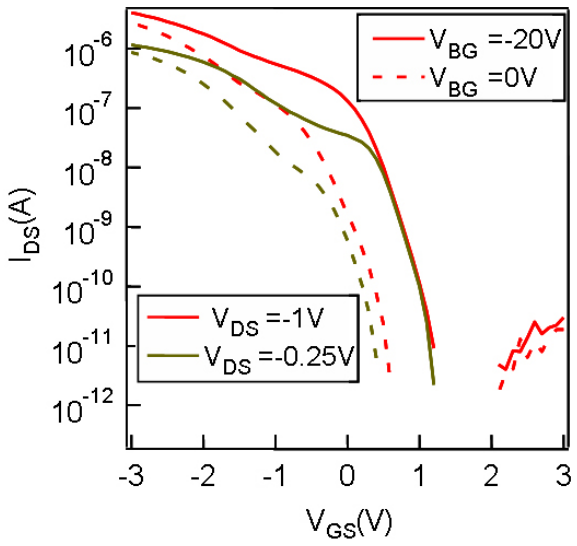

Figure S1. **Drain current vs. top-gate voltages at different bottom gate potentials.** When the top-gate has been deposited, bottom gate modulation is limited and the device is dominated by the top gate. V_{BG} is the applied back-gate voltage.

Literature for Supporting Information

1. Sze, S. M., *Physics of semiconductor devices*. ed.; Wiley: New York, 1981; 'Vol.' p.

[1] Sze, S. M., *Physics of semiconductor devices*. ed.; Wiley: New York, 1981.

[2] Appenzeller, J.; Lin, Y.-M.; Knoch, J.; Avouris, P. *Phys. Rev. Lett.* **2004,** 93, 196805.